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10/813,391	03/31/2004	Jae-Bon Koo	61610120US	7644

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EXAMINER	
ZUBAJLO, JENNIFER L	
ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
07/10/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Office Action Summary	Application No.	Applicant(s)	
	10/813,391	KOO ET AL.	
	Examiner	Art Unit	
	JENNIFER ZUBAJLO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/20/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claims 1, 3 and 7 the language of the claim is unclear. Claim 1 states: "A flat panel display, comprising: a plurality of pixels, where each of the plurality of pixels includes R, G and B unit pixels to embody red (R), green (G) and blue (B) colors, respectively, and where each of the unit pixels includes a transistor with multi gates, wherein transistors of at least two unit pixels of the R, G, and B unit pixels each include a offset region with a **different geometric structure** between the multi gates **from one another**."

The recitation of claim 4, last line "**different from one another**" is not clear.

It is not clear what **"different geometric structure"** is and needs to be further defined. It is not clear what **"from one another"** is referring to? Which one another? Therefore, dependent claims 2-8 are also rejected.

As to claim 9, "A flat panel display, comprising: a plurality of pixels, where each of the plurality of pixels including R, G and B unit pixels to embody red (R), green (G) and blue (B) colors, respectively, and where each of the unit pixels includes a transistor

with multi gates, wherein transistors of at least two unit pixels among the R, G, and B unit pixels each include an offset region having a **different resistance value** between the multi gates **from one another**." It is not clear what **"from one another"** is referring to? Which one another? Therefore, dependent claims 10-16 are also rejected.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 5 and 7 are rejected under 35 U.S.C. 102(b) as being unpatentable over Tsutomu Yamada (Patent No.: US 6,366,025) in view of Hsieh (US 6,670,230).

As to claim 1, Yamada teaches:

A flat panel display, comprising: a plurality of pixels, where each of the plurality of pixels includes R, G and B unit pixels to embody red (R), green (G) and blue (B) colors (see figure 3 and 5 element 160 (R, G, and B) and column 6 lines 53-54).

Yamada fails to directly teach the unit pixels with R, G, and B sub pixels, where each of the unit pixels includes a transistor with multi gates, wherein transistors of at least two unit pixels of the R, G, and B unit pixels each include a offset region with a different geometric structure between the multi gates from one another.

However, Hsieh is cited to teach that it is well known for a transistor to have a multi gates, wherein transistor of include a offset region with a different geometric

structure between the multi gates from one another (see, col.2, lines 37-46, col.3, lines 61-67, col.4, lines 38-44 Note: the Examiner broadly interoperate "the offset region between multi gates form one another" as the offset region between the dual gate and the " different geometric structure" as the thickness. As Examiner best understood).

Therefore, it would have been obvious to one skill in the art at the time of the invention was made to have incorporated Hsieh's transistor having multi gates with an offset region into Yamada's R, G, B sub- pixel transistor, so that Yamada's (RGB) sub-pixel transistors to have a of a multi gate with an offset region, because this will decrease the fabrication cost and reduce the leakage current.

As to claim 3 (dependent on claim 1), Yamada as modified by Hsieh teaches the limitations of claim 1 for the reasons above. Hsieh discloses that the lengths of the offset regions between the multi gates of the transistors of the unit pixels are the same (col.2, lines 37-4) and the offset lengths of a portion in the offset regions, where the portion is not doped with impurities, are different from one another (col.4, lines 38-44).

As to claims 5 and 7 (dependent on claim 1), Yamada as modified by Hsieh teaches the limitations of claim 1 for the reasons above. Hsieh discloses that the lengths of the offset regions between the multi gates of the transistors of the unit pixels are the same (col.2, lines 37-4) and the offset lengths of a portion in the offset regions, where the portion is not doped with impurities, are different from one another (col.4, lines 38-44).

5. Claims 9-11,13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsutomu Yamada (Patent No.: US 6,366,025) in of view Hsieh (6,670,230) and Ma et al (6,404,030)

As to claim 9, Yamada teaches a plurality of pixels, where each of the plurality of pixels includes R, G and B unit pixels to embody red (R), green (G) and blue (B) colors (see figure 3 and 5 element 160 (R, G, and B) and column 6 lines 53-54).

Yamada fails to directly teach the unit pixels with R, G, and B sub pixels, where each of the unit pixels includes a transistor with multi gates, wherein transistors of at least two unit pixels of the R, G, and B unit pixels each include a offset region with a different geometric structure between the multi gates from one another.

However, Hsieh is cited to teach that it is well known for a transistor to have a multi gates, wherein transistor of include a offset region with a different geometric structure between the multi gates from one another (see, col.2, lines 37-46, col.3, lines 61-67,, col.4, lines 38-44 Note: the Examiner broadly interoperate "the offset region between multi gates form one another" as the offset region between the dual gate and the " different geometric structure" as the thickness. As Examiner best understood).

Therefore, it would have been obvious to one skill in the art at the time of the invention was made to have incorporated Hsieh's transistor having multi gates with an offset region into Yamada's R, G, B sub- pixel transistor, so that Yamada's (RGB) sub-pixel transistors unit to have a of a multi gate with an offset region, because this will decrease the fabrication cost and reduce the leakage current.

Yamada as modified by Hsieh don't teach an offset region having a different resistance value between the multi gates from one another.

Ma et al (hereinafter Ma) teaches a gate fingers (multi gates) transistor device in which the gate fingers (multi gates) having a different resistance value (see, col.3, line 41-51, col.4, lines 15-20).

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Ma's teachings of a gate fingers (multi gates) having a different resistance value with Yamada's (as modified by Hsieh) RGB pixel unit with an offset region between each gates, since this will give a rise to improve a high frequency performance of the semiconductor devices (see, col.2, lines 1-5).

As to claim 10 (dependent on claim 9), Yamada teaches the limitations of claim 9 for the reasons above.

Yamada doesn't teach the unit pixels having different resistance values from one another each include light-emitting device, respectively, and the transistors for controlling currents supplied to the light-emitting device of each unit pixel.

Ma teaches the unit pixels having different resistance values from one another each include light-emitting device, respectively, and the transistors for controlling currents supplied to the light-emitting device of each unit pixel (see column 2 lines 9-40, column 5 lines 24-29, and figure 6).

None of the references directly teach having channel layers with the same size however it would have been obvious matter of design choice since applicant has not

disclosed channel layers of the same size solving any stated problem and it appears that channel layers of different sizes would perform equally well.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yamada with the different resistance values and the transistors for controlling currents taught by Hsieh and Ma to maintain even light emission intensity.

As to claim 11, Yamada as modified by Hsieh teaches the limitations of claim 1 for the reasons above. Hsieh discloses that the lengths of the offset regions between the multi gates of the transistors of the unit pixels are the same (col.2, lines 37-4) and the offset lengths of a portion in the offset regions, where the portion is not doped with impurities, are different from one another (col.4, lines 38-44).

As to claims 13 and 15 (dependent on claim 1), Yamada as modified by Hsieh teaches the limitations of claim 1 for the reasons above. Hsieh discloses that the lengths of the offset regions between the multi gates of the transistors of the unit pixels are the same (col.2, lines 37-4) and the offset lengths of a portion in the offset regions, where the portion is not doped with impurities, are different from one another (col.4, lines 38-44).

Allowable Subject Matter

1. Claims 2, 4,6,8 12,14 and 16 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

2. The following is an examiner's statement of reasons for allowance: the cited prior arts has failed to teach applicant's claimed invention "*where an offset length of an offset region of a transistor for driving a light-emitting device having the highest luminous efficiency among the transistors is longer than an offset length of an offset region of transistors for driving light-emitting devices having relatively lower luminous efficiency*".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

6. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Patent Nos.: US 7,163,848 and US 7,053,890.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JENNIFER ZUBAJLO whose telephone number is (571)270-1551. The examiner can normally be reached on Monday-Friday, 8 am - 5 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jennifer Zubajlo/
4/23/08

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629